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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,506	11/03/2006	Reinhard Weiberle	10191/4200	7470

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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,506	WEIBERLE ET AL.	
	Examiner	Art Unit	
	Bryce P. Bonzo	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/17/07, 10/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-15 are cancelled.

Claims 16-19 and 26 are rejected under 35 USC §102.

Claims 20-25 and 27-30 are rejected under 35 USC §103.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-19 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Quach (United States Patent No. (6,640,313 B1). As per the claims:

16. A program-controlled computer unit, comprising:

a single controller core (column 4, lines 28-34) including at least a first execution unit and a second execution unit (column 4, lines 37-39);

wherein the first and the second execution units are operable independently of one another in a first operating mode (column 4, lines 20-23), and wherein the first and

the second execution units are operable in a second operating mode to process the same set of instructions in parallel (column 4, lines 18-20).

17. The program-controlled computer unit as recited in claim 16, further comprising:

an error detection device that performs, in the second operating mode, at least one of an error detection and an error correction in accordance with an error handling routine (column 8, lines 9-16).

18. The program-controlled computer unit as recited in claim 17, wherein the error detection device includes a coder that provides at least one of: a) an error detection code to input data conveyed to the first and the second execution units on the input side; and b) an error correction code to an output signal calculated by at least one of the first and the second execution units (column 12, lines 5-64).

19. The program-controlled computer unit as recited in claim 18, wherein the error detection device includes a first comparison unit downstream from the first and the second execution units on the output side, and wherein the first comparison unit provides a comparison, in accordance with an error handling routine, for at least one of the following: a) a set of output signals calculated by the first and the second execution units; and b) a set of error correction codes assigned to output signals calculated by the first and the second execution units, whereby it is determined whether an error is

present, and wherein an error signal is output in the event an error is present (column 12 in its entirety).

26. A method for operating a program-controlled computer unit that includes: a) a single controller core (column 4, lines 28-34) having at least a first execution unit and a second execution unit (column 4, lines 37-39), wherein the first and the second execution units are operable independently of one another in a first operating mode (column 4, lines 20-23), and wherein the first and the second execution units are operable in a second operating mode to process the same set of instructions in parallel (column 4, lines 18-20); and b) an error detection device having at least one comparison unit (column 6, lines 1-7), the method comprising:

performing, in the second operating mode, at least one of an error detection and an error correction in accordance with an error handling routine using the error detection device (column 8, lines 9-16), wherein the at least one comparison unit provides a comparison, accordance with an error handling routine, for at least one of the following: a) a set of input data for the first and the second execution units; b) a set of output signals calculated by the first and the second execution units; and c) a set of error correction codes assigned to output signals calculated by the first and the second execution units, and wherein an error signal is generated if the comparison does not produce an agreement (column 12, in its entirety).

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach (United States Patent No. 6,640,313 B1).

As per claim 20, Quach discloses:

20. The program-controlled computer unit as recited in claim 19, wherein the error detection device includes a second comparison unit upstream from at least one of the first and the second execution units on the input side, the second comparison unit comparing input data conveyed to at least one of the first and the second execution units on the input side with input data provided with *an error detection code*, in accordance with an error detection routine, to determine whether an error is present, and wherein an error signal is output in the event an error is present (column 12).

Quach does not disclose the use of checksums as the error detection code. Official Notice is given that the checksum is a well known error detection scheme used in computer processing. Checksums offer lightweight error detection. Systems which simply drop corrupted data or simply count error benefit greatly from checksums, as they provide a simple and computationally inexpensive error detection code. Further, as the checksum can be used a precursor for parity calculations, it allows systems have

built near-compatibility with parity error correction codes. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to implement the error detection portion of Quach as a checksum, thus allowing the comparison of stages within a processing system to be handled in a computationally efficient manner.

21. The program-controlled computer unit as recited in claim 20, further comprising:

at least one data register associated with at least one of the first and the second execution units, wherein the at least one data register is connected on the output side to both the inputs of the first and the second execution units and to the second comparison unit, and wherein input data for at least one of the first and the second execution units are stored in the at least one data register (column 13, lines 2-10).

22. The program-controlled computer unit as recited in claim 20, further comprising: a shadow register, wherein input data most recently conveyed to at least one of the first and the second execution units prior to calculation are stored (column 11, line 8 through column 12, line 4).

23. The program-controlled computer unit as recited in claim 22, wherein the shadow register is a first-in-first-out register (column 11, line 8 through column 12, line 4).

24. The program-controlled computer unit as recited in claim 22, further comprising:

a control device coupled on the input side to the error detection device and coupled on the output side to the shadow register (column 11, lines 8 though column 12, line 4), wherein the control device generates an enabling signal for enabling the shadow register only if no error is detected by the error detection device (column 11, lines 35-38).

25. The program-controlled computer unit as recited in claim 24, wherein the program-controlled computer unit is one of a microcontroller and a microprocessor (column 1, lines 20-33).

As per claim 27, Quach does not explicitly disclose:

wherein different error signals are generated for different types of error.

Quach does disclose the handling of two different kinds of errors , data transmission errors and data processing errors inside various functional units. Further Quach discloses different error handling depending on the source of the error. Additionally, Quach's use of the parity error correction handles one of those error sources better than the other. Official Notice it is given to use multiple signals to indicate multiple types of error. This allows the system to handle the errors differently. For instance, an unrecoverable data corruption can be flagged as such leading to data

being dropper, while unmatched parallel can be flagged to indicate re-execution is needed. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to implement the use of multiple error signals into the system of Quach, thus allowing for the clear transition from one form of error handling to another, thus allowing for a more robust and effective error response.

28. The method as recited in claim 27, wherein the input data are first conveyed to both the first and the second execution units, and subsequently corresponding error correction codes are generated from the input data (column 12, lines 5-42).

29. The method as recited in claim 28, wherein stored input data of the previous calculation are overwritten only if one of: a) a comparison of the stored input data; and b) a comparison of output result data calculated from the stored input data, does not result in an error signal (column 11, lines 35-58).

30. The method as recited in claim 29, wherein the output result data calculated from the stored input data are transmitted for only if an error signal is not present (column 11, lines 35-58).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bryce P Bonzo/
Primary Examiner, Art Unit 2113